REMARKS

The Specification is herein amended, Claims 1-5 are herein canceled, without prejudice, Claims 14-21 are herein either actually or constructively amended, the Abstract is herein amended, and the Drawing is herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims would have been allowable as originally filed. Both "marked-up" and "clean" versions of each the Specification, the Claims, and the Abstract are herewith submitted. A substitute formal drawing Sheet 6/6 is also herewith submitted. Therefore, reconsideration of the present application in light of the foregoing amendment after final rejection and these remarks is respectfully requested.

Substitute Formal Drawing:

The Applicants request that the Examiner kindly accept the herewith submitted substitute formal drawing Sheet 6/6 (Fig. 6.0) showing the corrected leader line position for the spacer 18. No new matter has been introduced.

Rejection of Claims 1-5 and 14-21 under 35 U.S.C. §103(a):

The Examiner has rejected Claims 1-5 and 14-21 under 35 U.S.C. §103(a) as being unpatentable over Su et al. (US 6,133,096), in view of Cho et al. (US 6,027,971), stating:

> ... claims 1, 2, 4, 14, 15, 19, Su ... discloses a semiconductor memory device comprising: a silicon substrate (1) (... col. 3, ll. 38-40) including a peripheral memory region (90) and a core memory region (70); a transistor formed on the peripheral memory region; one set of dual gate core memory structures (15) including a stacked layer arrangement of semiconductor layers (7, 10) and a dielectric material layer (9), the dual gate core memory structure having sidewall portions; sidewall spacer structures (21) of silicon nitride (... col. 6, ll. 13-18) formed on the sidewall portions of [the] dual gate core memory structures (Fig. 7B; Fig. 15).
>
> **Su ... does not explicitly teach that the silicon nitride for forming [the] spacer structures (21) [has] the chemical formula of Si_3N_4.**
>
> Cho ... discloses a semiconductor memory device comprising: a dual gate core memory structure (62) formed in the core memory region; [] sidewall spacer structures (68) formed on sidewall portions of the dual gate core memory structures, **wherein the sidewall spacer structure [is] formed [from] silicon nitride (Si_3N_4). ... obvious ... to form sidewall spacer structures of silicon nitride (Si_3N_4) as taught by Cho ....**
>
> ... inherent that, the sidewall spacer structures in above combined device is also capable [of protecting] the stacked layer arrangement during etching operations and is compatible with ion implantation and salicidation fabrication process[es] as [the] claimed device.
>
> ... claimed properties [or] functions are presumed to be inherent. In re Best, 195 USPQ 430, 433 (CCPA 1977).
>
> The expressions "dual-purpose" and "being used for lithographic patterning for protecting said stacked layer arrangement during etching operations" [in] claims 1, 4, 14, 17, 19,

> and 21[,] are considered as intended use limitations and are not considered towards patentability. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to [patentably] distinguish the claimed invention from the prior art. ....
>
> ... claims 3, 5, 17, 18, Su ... teaches that the silicon nitride spacer structures (21) being deposited in a thickness of 1000 [Å] (col. 6, ll. 13-18).
>
> ... claims 20 and 21, ... Su ... the silicon nitride spacer also being a pattern formation structure for at least one peripheral memory element [(Fig. 15)].

Claims 1-5 are herein canceled, without prejudice, thereby rendering moot their grounds for rejection. Remaining independent Claims 14, 17, 19, and 21 are herein amended to better recite the ARC materials and their critical thickness range. Claims 15, 16, 18, and 20 now subsume the limitations from the herein amended claims from which they respectively depend.

Notwithstanding Claims14-21 being herein amended to better encompass the present invention, the Applicants respectfully traverse the Examiner's ground for rejection on this basis. As conceded by the Examiner, "Su ... does not explicitly teach that the silicon nitride for forming [the] spacer structures (21) [has] the chemical formula of Si_3N_4." Su merely teaches (col. 6, ll. 13-18): "**Insulator spacers 21**, comprised of **silicon nitride**, are next formed on the sides of the gate structure, in peripheral device region 90, and on the sides of stacked gate structures 15, in flash memory cell region 70. ... **at a thickness between about 1000 to 2500 Angstroms**, ..." [Emphasis added.] Su's spacer 21 is, thus, too thick to provide the presently claimed anti-reflectance capability. As such, Su does not teach, suggest, nor motivate the presently claimed ARC materials (i.e., **SiON, stoichiometric Si_3N_4, or SiGe** in the Markush group) nor the presently claimed **thickness range from 300 Å up to 1000 Å.**

The Examiner has combined Cho with Su in order to show stoichiometric silicon nitride (Si_3N_4) as a sidewall material: "Cho ... discloses a semiconductor memory device comprising: a dual gate core memory structure (62) formed in the core memory region; [] sidewall spacer structures (68) formed on sidewall portions of the dual gate core memory structures, wherein the sidewall spacer structure [is] formed [from] silicon nitride (Si_3N_4). ... obvious ... to form sidewall spacer structures of silicon nitride (Si_3N_4) as taught by Cho ...." Cho merely teaches (col. 4, ll. 40-43): "... the **insulating spacers 68** are preferably formed of a material having a large etching selectivity relative to silicon dioxide, such as a nitride material, including **silicon nitride (Si_3N_4) and silicon oxynitride (SiON)**." [Emphasis added.] Cho does **not** teach any thickness range at all for the spacers 68. As such, Su, even in view of Cho, does not teach, suggest, nor motivate the presently claimed ARC materials (i.e., **SiON, stoichiometric Si_3N_4, or SiGe** in the Markush

group) nor the presently claimed **thickness range from 300 Å up to 1000 Å.**

In contrast to Su, in view of Cho, the present invention teaches and claims **a sidewall spacer structure 18** comprising **an anti-reflective coating material** for protecting said stacked layer arrangement during etching operations, **wherein said anti-reflective coating material comprises a material selected from a group consisting of *silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe)***, said group being compatible with ion implantation and salicidation fabrication processes, and **wherein said anti-reflective coating material comprises a thickness ranging from *300 Å up to 1000 Å*** and also comprises a pattern formation structure for said at least one peripheral memory element (Specification, paras. 6, 9, and 11; herein amended Claim 21). Neither Su nor Cho teach the use of **SiGe** as a spacer material at all. As such, the present invention claims Markush species (i.e., **SiON, stochiometric Si_3N_4, and SiGe**) as well as a **critical thickness range (i.e., ≥300 Å and <1000 Å)** which are not taught, suggested, nor motivated by Su, even in view of Cho. For anti-reflection or optical absorption, only the present invention spacers 18 provide the critical thickness range. While Su and Cho disclose typical spacers, such spacers do not provide the superior absorption capability as do those of the present invention (i.e., not all spacers are created equally).

Specifically, the physics of the present invention may be described as follows:[1]

> No material is perfectly transparent; as light passes through any optical medium (except vacuum) its energy is partially absorbed, increasing the internal energy of the material, and the intensity (power per unit area) is correspondingly attenuated.
>
> **When a beam of light passes through a *thin* sheet of material, of thickness *dx*, the decrease *dI* in its intensity *I* is found to be proportional to the initial intensity *I* and to the thickness *dx*.** Thus[,]
>
> $$dI = -\alpha I dx. \qquad (38\text{-}6)$$
>
> The proportionality constant α, which depends on the material, is called the *absorption coefficient*. The intensity after passage through a slab of finite thickness x can be obtained by integrating Eq. (38-6):
>
> $$I = I_0 e^{-\alpha x}, \qquad (38\text{-}7)$$
>
> where I_0 is the intensity at x = 0. Equation (38-7) is called *Lambert's law*. [Emphasis added.]

This being so, where the initial intensity and the absorption coefficient are constant, by

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1. Francis W. Sears, Mark W. Zemansky, and Hugh D. Young, University Physics, 5th Ed., pp. 648-649, Addison-Wesley Publishing Company (June 1980).

lowering the coating thickness (i.e., *dx* decreasing), the intensity is also lowered (i.e., *dI* decreasing), because *dI* is directly proportional to *dx* (Eq. 38-6). Conversely, if the thickness increases, so does the intensity, thereby resulting in undesirable reflectance, the very problem illustrated by the cited art for which the present invention provides a solution. Further, the thickness for minimizing specular reflectance (i.e., maximizing absorption) may be expressed as follows:[2] $t = m/[2(n^2\text{-}\sin^2 f)^{1/2}Dn]$, where m = number of fringes, n = the refractive index, f = the incident angle, and Dn = the wavenumber span (wavenumber = 1/wavelength). Consequently, the Applicants have claimed their critical thickness range **(i.e., ≥300 Å and <1000 Å)** in combination with their claimed ARC materials (i.e., **SiON, stochiometric Si_3N_4, and SiGe**) for providing a spacer material 18 having **superior optical absorption** capability, *during photoresist processing as well as during subsequent ion implantation and salicidation fabrication processing.*

In particular, only the present invention comprises an ARC which approaches total internal reflection as given by the following equation derived from Huygen's Principle and Snell's Law:[3] $\sin \phi_{crit} = n_b/n_a$, where n_b = the refractive index of the medium through which the incident light (wave front) travels prior to entering the ARC (e.g., $n_b = 1$ in the case of air)[4], n_a = the refractive index of the ARC itself (e.g., $n_a \approx 1.5$ for SiON,[5] $n_a \approx 2.0$ for Si_3N_4,[6] and $n_a \approx$ 3.4 to 4.0 for SiGe depending on exact stoichiometry[7]), and ϕ_{crit} = the critical angle at which total internal reflection occurs. Sears et al. further explain: "Total internal reflection can occur only when a ray is incident on the surface of a medium whose index is smaller than that of the medium

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2. www.piketech.com: "Film Thicknesses and Composition," Pike Technologies website, (December 16, 2002).

3. Sears et al., pp. 657-658.

4. *Id.*, at 657.

5. www.ads.computer.org/proceedings/pi/0440/0440015abs.html: G. L. Bona et al., "Versatile Silicon Oxynitride Planar Lightwave Circuits for Interconnect Applications," IEEE 6th Annual International Conference on Parallel Interconnects, Anchorage, Alaska, (October 17-19, 1999).

6. www.ai.mit.edu/people/tk/tks/silicon-nitride.html (December 17, 2002).

7. www.ncsr.csci-va.com/ncsr/materials/sige.asp (December 17, 2002).

in which the ray is traveling."[8]

Further, Sears et al. explain destructive interference for thin films: "It follows that if the film thickness is 1/4 wavelength in the film (normal incidence is assumed), the light reflected from the first surface [i.e., the ARC surface in the present invention] will be 180 out of phase with that reflected from the second [i.e., the gate polysilicon surface in the present invention], and complete destructive interference will result. The thickness can, of course, be 1/4 wavelength for only one particular wavelength."[9]

As such, the presently claimed device having the **critical thickness range** allows operation not only during **photoresist development** processes (e.g., using ultraviolet light either in the **UV ultraviolet wavelength range of 100 nm to 250 nm** or the **DUV wavelength range of 4 nm to 100 nm**)[10] ***but also*** during **ion implantation and salicidation** (e.g., using laser light in the **violet visible range of about 420 nm** for nitrogen E-beam or ion-beam laser)[11], wherein the present invention advantage lies. Typically, low-energy laser-beams are used for alignment marking[12], ion-beam lasers for defect repair[13], inspection[14], and package marking[15]. Thus, the present invention ARC protects the device during any subsequent processing steps using a UV source as well as a low-end visible range low-energy laser.

The present invention, comprising an ARC in the claimed critical thickness range (**≥ 300 Å and <1000 Å, i.e., ≥ 30 nm and <100 nm**), when practiced by forming a spacer 18 comprising the ARC at a thickness of 30 nm, **approaches almost complete destructive interference in the low-end UV range or the high-end DUV range**, because **the claimed low-end ARC thickness of 30 nm is approximately equal to 1/4 of the low-end UV wavelength**

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8. Sears et al., p. 657.

9. Sears et al., pp. 715-716.

10. Peter Van Zant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing," 4th Ed., p. 205 (McGaw-Hill, 2000).

11. CRC Handbook, p. 10-222.

12. Van Zant, p. 236.

13. *Id.*, at 277.

14. *Id.*, at 451.

15. *Id.*, at 580.

or the high-end DUV wavelength of 100 nm, which would then be 25 nm. At the other end of the spectrum, so to speak, the present invention, when practiced by forming a spacer 18 comprising the ARC at a thickness of <100 nm, **also approaches almost complete destructive interference in the low-end laser range**, because **the claimed high-end ARC thickness of <100 nm is approximately equal to 1/4 of the low-end nitrogen ion beam laser wavelength of 420 nm**, which would then be 105 nm).

Consequently, the Applicants respectfully submit that the claimed spacer 18 (ARC) thickness (i.e., thinness, "less is more" in the present invention) range (**≥ 300 Å and <1000 Å, i.e., ≥ 30 nm and <100 nm**) is not arbitrary and has been purposefully selected by the Applicants in order to form a patentably distinct spacer being operational during many facets of device fabrication. The pending claims are herein amended to demonstrate the patentably distinct structural limitations which are not taught, motivated, suggested, nor even inherent in the cited art. Thus, Su, even in view of Cho, does not teach, motivate, nor suggest herein amended independent Claims 14, 17, 19, and 21, respectively reciting:

14. **(Amended)** A semiconductor memory device, comprising:
    a. a silicon substrate;
    b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;
    c. a core memory region also delineated on said substrate,
    said core memory region having at least one set of dual gate core memory structures thereon formed,
    said dual gate core memory structures comprising a stacked layer arrangement, and
    said stacked layer arrangement comprising:
    a semiconductor material; and
    a dielectric material defining respective sidewall portions; and
    d. **a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, said anti-reflective coating material comprising silicon germanium (SiGe).**
    [Emphasis added.]

17. **(Amended)** A semiconductor memory device, comprising:
    a. a silicon substrate;
    b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;
    c. a core memory region also delineated on said substrate,
    said core memory region having at least one set of dual gate core memory structures thereon formed,
    said dual gate core memory structures comprising a stacked layer arrangement, and
    said stacked layer arrangement comprising:
    a semiconductor material; and
    a dielectric material defining respective sidewall portions; and

d. **a sidewall spacer structure comprising an anti-reflective c ating material for protecting said stacked layer arrangement during etching operations, wherein said anti-reflective coating material c mprises a thickness ranging from 300 Å up t 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least ne peripheral memory element.** [Emphasis added.]

19. **(Amended)** A semiconductor memory device, comprising:
a. a silicon substrate;
b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;
c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising a stacked layer arrangement, and
said stacked layer arrangement comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions; and
d. **a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, wherein said anti-reflective coating material comprises silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and**
wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least one peripheral memory element. [Emphasis added.]

21. **(Amended)** A semiconductor memory device, comprising:
a. a silicon substrate;
b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;
c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising a stacked layer arrangement, and
said stacked layer arrangement comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions; and
d. **a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said group being compatible with ion implantation and salicidation fabrication processes, and**
wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least one peripheral memory element. [Emphasis added.]

As such, Su, even in view of Cho, does not teach, suggest, nor motivate Claims 15, 16, 18, and 20, now subsuming the limitations of the herein amended independent claims. Therefore, the

Applicants respectfully request that the Examiner's ground for rejection on this basis be withdrawn.

CONCLUSION

Accordingly, the Specification is herein amended, Claims 1-5 are herein canceled, without prejudice, Claims 14-21 are herein amended, the Abstract is herein amended, and the Drawing is herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims would have been allowable as originally filed. Both "marked-up" and "clean" versions of each the Specification, the Claims, and the Abstract are herewith submitted. A substitute formal drawing Sheet 6/6 is also herewith submitted. Therefore, reconsideration of the present application in light of the foregoing amendment after final rejection and these remarks is respectfully requested. ***The Examiner is further cordially invited to telephone the undersigned for any reason which would advance pending claims to allowance.***

Respectfully submitted,

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MARKED-UP VERSION OF THE SPECIFICATION

In the Specification: Kindly accept the substitute Specification as follows, amended for paragraph numbering, style, and clarity. No new matter has been introduced.

PATENT
Docket No. P1025

PATENT APPLICATION

DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES [AND METHOD OF FORMING]

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CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application is related to co-pending U.S. Provisional Patent Application Ser. No. 60/159,235, also entitled "DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING["],"_ filed October 13, 1999.

TECHNICAL FIELD

[0002] The present invention relates to integrated semiconductor circuits and anti-reflective coating fabrication techniques used in dual gate semiconductor technology, such as [FLASH] flash memory technology. More particularly, the present invention relates to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of the transistor gates used in dual gate semiconductor technology, such as [FLASH] flash memory technology. Even more particularly, the present invention relates to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of transistor gates in the core memory region as used in dual gate semiconductor technology, such as [FLASH] flash memory technology.

BACKGROUND OF THE INVENTION

[0003] Dual gate technology, such as [FLASH] flash memory technology, uses anti-reflective coatings to ease lithographic patterning. The closely formed dual gate transistor gates require electrical isolation provided by spacers formed on the sidewall structure of the gate stacks. Typically, a dielectric material, similar to the anti-reflective coating material, is used to form the spacers on the sidewall structure of the dual transistor gates. According to known fabrication techniques, the anti-reflective coating is used twice during formation of the spacers, which, as a result of etching and stripping action of the fabrication process, the thickness of the anti-reflective coating is reduced, resulting in a loss of the effectiveness of the anti-reflective coating. Thus, there is seen to exist a need for a fabrication technique that does not depend on deteriorated use of the anti-reflective coating to fabricate the sidewall spacers of dual gate semiconductor devices.

BRIEF SUMMARY OF THE INVENTION

[0004] Accordingly, the present invention provides a dual gate semiconductor device, such as a [FLASH] flash memory semiconductor device, whose plurality of dual gate sidewall spacer structures [are] is not formed from traditional dielectric material similar to the anti-reflective coating material that is traditionally used for lithographic patterning. Rather, the present invention provides a dual gate semiconductor structure whose sidewall spacers are formed by a first and second anti-reflection fabrication process, whereby[,] the sidewall spacers of the dual transistor gate structure in the core memory region are left coated with the second anti-reflective coating material, such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), or other material having optical properties compatible with subsequent fabrication processing, to form sidewall spacers for use in subsequent implant and salicidation steps, commonly used during fabrication of the semiconductor device being formed. Other features of the present invention are disclosed or are apparent in the section entitled "DETAILED DESCRIPTION OF THE INVENTION."

BRIEF DESCRIPTION OF DRAWINGS

[0005] The invention, including its various [objects,] features[,] and advantages, may be more readily understood with reference to the following detailed description of the best mode for

carrying out the invention, taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, as below-referenced. Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

1. Figure 1 is a cross-sectional view of a prior art semiconductor device shown at a fabrication stage whereby anti-reflective coating portions overlying various memory element regions will be subjected to various etching process steps after patterning.

2. Figure 2 is a cross-sectional view of a semiconductor substrate shown at a fabrication stage in accordance with the present invention where a first anti-reflective coating has been utilized for patterning core and periphery substrate regions.

3. Figure 3 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 2 shown with the first coat of anti-reflective coating [has] having been removed.

4. Figure 4 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 3 shown at a fabrication stage where a second anti-reflective coating [have] has been formed over the patterned core and peripheral regions in accordance with the present invention.

5. Figure 5[.] is a cross-sectional view of the memory semiconductor substrate depicted in Figure 4 shown having patterned peripheral memory regions and core memory regions fully coated with the second anti-reflective coating.

6. Figure 6 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 6 shown having sidewall spacers formed from the second anti-reflective coating in accordance with the present invention.

[Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.]

DETAILED DESCRIPTION OF THE INVENTION

[0006] Figure 1 is a cross-section of a prior art semiconductor substrate 10 shown at an early fabrication stage for forming a flash memory device 100. As depicted, substrate 10 comprises a core region 10C and a periphery region 10P. The core memory stacks 12, 13 and periphery memory region 9 are provided with an anti-reflective coating 14 having a typical thickness *d* in a range of [300Å to 1000Å] 300 Å to 1000 Å. Core memory stacks 12, 13, at this stage of

fabrication[,] and as depicted in Figure 1, may comprise a thin layer of silicon dioxide 11, a first polysilicon layer P1, a dielectric layer D1 over layer P1 and a second polysilicon layer P2 over layer D1. The spacing S between stacks 12 and 13 is in the sub-micron range which necessitates the formation of spacers between stacks 12 and 13 to protect the corner regions 11a of the silicon dioxide layers 11 during various etching operations. The peripheral memory region 9 may comprise, as depicted in Figure 1, a layer of polysilicon material P2 for use in formation of the periphery memory elements. Further, as previously discussed, the prior art processes utilize anti-reflective coatings 14 multiple times, in combination with a photoresist material R, for use in formation of resist patterns, such as resist patterns 15, [and] 16.

[0007] Figure 2 shows a flash memory device 200, in accordance with the present invention, at a fabrication stage where, rather than applying photoresist material[,] to form subsequent other resist patterns, the first anti-reflective coating layers 14 are used only to form the core memory stacks 12, [and] 13 and the peripheral memory region 9.

[0008] Accordingly, Figure 3 shows the device 200 with anti-reflective coating 14, depicted in Figure 2, stripped from the core memory stacks 12, [and] 13 and the peripheral memory region 9.

[0009] Figure 4 shows the present invention, where, in preparation for subsequent patterning processes, a second coating of anti-reflective coating material 17, such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), or other suitable material with dual purpose optical properties compatible with other fabrication processes, is deposited in a thickness in a range of [300Å to 1000Å] 300 Å to 1000 Å over the core memory stacks 12, [and] 13, the spacing S between stacks 12, [and] 13, floor region F, the core-periphery interface region CP, and over the periphery memory region 9.

[0010] As shown in Figure 5, the second coating 17 is used for patterning any remaining gate structures, such periphery gate structures 7, [and] 8 in the periphery memory region 9, depicted in Figure 4, by appropriate masking and etching operations.

[0011] Figure 6 shows the present invention where spacers 18 are defined on the sidewalls of the core memory gate structures 12, [and] 13 after stripping the second anti-reflective coating 17 from over the second polysilicon layers P2 of core memory gate stacks 12, [and] 13, and from over the periphery memory gate structures 7, [and] 8. Accordingly, the present invention provides a dual gate semiconductor structure 200 whose sidewall spacers 18 of core memory gate

structures 12, [and] 13 are formed by a first and second anti-reflection fabrication process. In accordance with the present invention, the sidewall spacers 18 of the dual transistor gate structure in the core memory region are left coated with the second anti-reflective coating material, such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), or other material having optical properties compatible with subsequent fabrication processing, to form sidewall spacers for use in subsequent implant and salicidation steps, commonly used during fabrication of the semiconductor device.

[0012] Information, as herein shown and described in detail, is fully capable of attaining the above-described [object] advantages of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference[. And] and are intended to be encompassed by the present claims.

[0013] Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. §112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

MARKED-UP VERSION OF THE CLAIMS

In the Claims:

A. Kindly cancel Claims 1-5, without prejudice.

B. Kindly amend Claims 14-21, as follows.

14. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed [thereon];

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed [thereon],

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising: [of]

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. [an anti-reflective coating material serving a dual-purpose of being a sacrificial coating structure for lithographic patterning and as] a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, said anti-reflective coating material comprising silicon germanium (SiGe).

15. **(Amended)** A semiconductor memory device, as recited in Claim 14,

wherein[:] said anti-reflective coating material [being] further comprises a material selected from [an anti-reflective coating material] a group consisting of silicon oxynitride (SiON)[,] and silicon nitride (Si_3N_4)[, and silicon germanium (SiGe)], and

wherein said [material] group [having anti-reflective optical properties and being] is compatible with ion implantation and salicidation fabrication processes.

16. **(Amended)** A semiconductor memory device, as recited in Claim 15, wherein[:] said anti-reflective coating material [being deposited in] comprises a thickness ranging from [300Å to 1000Å] 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and[,] also [being] comprises a pattern formation structure for said at least one peripheral memory element.

17. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed [thereon];

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed [thereon],

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising:

a [of] semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. [an anti-reflective coating material serving a dual-purpose of being a sacrificial coating structure for lithographic patterning and as] a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, wherein said anti-reflective coating material [being deposited in] comprises a thickness ranging from [300Å to 1000Å] 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and[,] also [being] comprises a pattern formation structure for said at least one peripheral memory element.

18. **(Amended)** A semiconductor memory device, as recited in Claim 17,

wherein[:] said anti-reflective coating material [being] comprises a material selected from [an anti-reflective coating material] a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), and

wherein said [material] group [having anti-reflective optical properties and being] is compatible with ion implantation and salicidation fabrication processes.

19. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed [thereon];

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed [thereon],

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising: [of]

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. [an anti-reflective coating material serving a dual-purpose of being a sacrificial coating structure for lithographic patterning and as] a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations,

wherein said anti-reflective coating material [being] comprises [selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and] silicon germanium (SiGe)[, said material group having anti-reflective optical properties and] being compatible with ion implantation and salicidation fabrication processes[.] and

wherein said anti-reflective coating material [being deposited in] comprises a thickness ranging from [300Å to 1000Å] 300 Å up to 1000 Å (i.e., ≥300 Å and ≤1000 Å) and[,] also [being] comprises a pattern formation structure for said at least one peripheral memory element.

20. **(Amended)** A semiconductor memory device, as recited in Claim 19,

wherein said anti-reflective coating material further comprises a material selected from a group consisting of silicon oxynitride (SiON) and silicon nitride (Si_3N_4), and wherein said group is compatible with ion implantation and salicidation fabrication

processes.

[wherein said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å and, also being a pattern formation structure for said at least one peripheral memory element.]

21. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed [thereon];

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed [thereon],

said dual gate core memory structures comprising a stacked layer arrangement, and [of]

said stacked layer arrangement comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. [an anti-reflective coating material serving a dual-purpose of being a sacrificial coating structure for lithographic patterning and as] a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations,

wherein said anti-reflective coating material [being] comprises a material selected from [an anti-reflective coating material] a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said [material] group [having anti-reflective optical properties and] being compatible with ion implantation and salicidation fabrication processes and,

wherein said anti-reflective coating material [being deposited in] comprises a thickness ranging from [300Å to 1000Å] 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and[,] also [being] comprises a pattern formation structure for said at least one peripheral memory element.

MARKED-UP VERSION OF THE ABSTRACT

In the Abstract: **Kindly amend the Abstract as follows. No new matter has been introduced.**

[DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING]

ABSTRACT OF THE DISCLOSURE

A dual gate semiconductor device, such as a [FLASH] flash memory semiconductor device, whose plurality of dual gate sidewall spacer structure is formed by a first and second anti-reflection fabrication process. The sidewall spacers of the dual transistor gate structures in the core memory region are left coated with the second anti-reflective coating material, after being used for gate patterning, to act as sidewall spacers for use in subsequent ion implant and salicidation fabrication steps. The second anti-reflective coating material is selected from a material group such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), or other anti-reflective coating material having optical properties and that are compatible with the subsequent implant and salicidation steps.

In the Drawings: **Kindly accept the herewith submitted substitute formal drawing Sheet 6/6 (Fig. 6.0) showing the corrected leader line position for the spacer 18. No new matter has been introduced.**